REMARKS

In an Office Action mailed on January 1, 2008, the Examiner: (1) rejected claims 11-34 under 35 U.S.C. § 102(b) as being anticipated by a publication entitled "The Nexus 5001 Forum Standard for a Global Embedded Processor Debug Interface, dated December 9, 1999 ("the Nexus Specification").

By this Amendment, Applicants cancel claims 28-34 without prejudice or disclaimer of the subject matter thereof. In addition, Applicants amend claims 11, 17-20 and 26 without prejudice or disclaimer of the subject matter thereof. Finally, Applicants present new claims 46-49. No new matter has been added.

Applicants respectfully request the Examiner to withdraw the rejection of claims 11-27 under 35 U.S.C. § 102(b) for at least the following reasons. To anticipate a reference must teach each and every limitation of the claim at issue. Concerning amended claim 11, the Nexus Specification does not anticipate claim 11 because it does not teach: "a plurality of functional circuit modules, each functional circuit module being clocked by a clock that represents a different time domain, such that the plurality of functional circuit modules operate independently of each other with respect to time and each of the plurality of functional circuit modules having timestamping circuitry, the timestamping circuitry providing a timestamping message that indicates a point in time when a predetermined event occurs in a corresponding time domain out of a plurality of time domains," as required by amended claim 11. In support of his position that the Nexus Specification teaches the claimed subject matter, the Examiner on page 3 of the Office Action states the following:

Nexus discloses "Multi-Processor: The Nexus standard allows for embedded processor implementations that comprise multiple clients to utilize a single AUX, depending upon the transfer bandwidth requirement for the application. The AUX may be designated for a single client or shared by multiple clients on the embedded device during runtime.

Messages transmitted via the AUX shall contain information defined by the Nexus standard indicating which client generated the message.")

Also note page 87-88, Table 7-2 and Table 7-3, *Independent clock allows for faster or slower transfer rate than with system clock reference.*

Based on the citation above, the Examiner concludes that the Nexus Specification teaches part of the subject matter recited in original claim 11. Although Applicants respectfully

disagree with the Examiner's conclusion, to expedite prosecution, Applicants have amended claim 11. Applicants respectfully submit that the Nexus Specification does not teach "each functional circuit module being clocked by a clock that represents a different time domain, such that the plurality of functional circuit modules operate independently of each other with respect to time and each of the plurality of functional circuit modules having timestamping circuitry, the timestamping circuitry providing a timestamping message that indicates a point in time when a predetermined event occurs in a corresponding time domain out of a plurality of time domains," as required by claim 11.

The Nexus Specification teaches the sharing of a single AUX port by "multiple clients." In this context, the Nexus Specification shows the following figure indicating an embedded processor that can interface with an external debugger using the AUX port.

Processor independent
Supports multiple on-chip
processors

Packet-Based Messaging

Program Trace
Data Trace
Memory Substitution
Vendor-Defined

Auxiliary Output

Debugger, Logic Analyzer,
Data Acquisition, Prototyping

1149.1 or Auxiliary Input
Parameter Tuning

IREE 1149.1 Protocol or Packet-based Messaging
Development Control and Status

Figure 4-1 illustrates Nexus development interface options for a class 2, 3 or 4 embedded processor.

Figure 4-1, page 13 of the Nexus Specification.

The Nexus Specification further describes the pin functions associated with the AUX port in Section 7, entitled "Auxiliary Port Signals" on pages 86-91. Relevant clock related portions of the Table 7-2, page 87, describe the Auxiliary Pin functions related to clocking aspects.

Read/Write Access to internal resources

Table 7-2 Auxiliary Pins

Auxiliary Pins	Description of Auxiliary Pins
мско	Message Clockout (MCKO) is a free-running output clock to development tools for timing of MDO and MSEO pin functions. MCKO can be independent of embedded processor system clock (CLOCKOUT). An embedded processor CLOCKOUT pin may be used as a functional equivalent for MCKO.

	Message Clockin (MCKI) is a free-running input clock from development tools for timing of MDI and MSEI pin functions. MCKI can be independent of the embedded processor
	system clock.

As evident from this description, the MCKO auxiliary pin relates to a free-running output clock, which can be independent of the embedded processor system clock (CLOCKOUT) and the MCKI auxiliary pin relates to a free-running input clock that can be independent of the embedded processor system clock. In sum, the Nexus Specification provides that one can either use the system clock or some other clock as the output clock on the MCKO auxiliary pin and the MCKI auxiliary pin.

Next, the Nexus Specification on page 88 notes the following:

Multi-Processor: The Nexus standard allows for embedded processor implementations that comprise multiple clients to utilize a single AUX, depending upon the transfer bandwidth requirement for the application. The AUX may be designated for a single client or shared by multiple clients on the embedded device during runtime. Messages transmitted via the AUX shall contain information defined by the Nexus standard indicating which client generated the message.

According to the Nexus Specification, a client is "[a] functional block on an embedded processor which will require development visibility and controllability. Examples are a central processing unit and an intelligent peripheral." (The Nexus Specification, Table 1-1, page 2). Based on this definition, the above paragraph merely states that the "embedded processor" may have multiple CPUs, for example, that can either share the AUX pins or not. The above paragraph further notes that the messages transmitted via the AUX shall have information "indicating which client generated the message." Applicants do not agree with the Examiner's conclusion that somehow the fact that the clock pins can receive a clock that is different from the system clock and the fact that there are multiple CPUs on the embedded processor means that the claimed subject matter is taught. In other words, the Nexus Specification does not teach:

"a plurality of functional circuit modules, each functional circuit module being clocked by a clock that represents a different time domain, such that the plurality of functional circuit modules operate independently of each other with respect to time and each of the plurality of functional circuit modules having timestamping circuitry, the timestamping circuitry providing a timestamping message that indicates a point in time when a predetermined event occurs in a corresponding time domain out of a plurality of time domains," as required by amended claim 11.

At best the Nexus Specification teaches that the messages transmitted via the AUX in a multi-client situation should include a client identifier type of information. That, however, is not the same as what is claimed. For at least the reasons given above, the Nexus Specification fails to teach each and every claim limitation of claim 11. Accordingly, Applicants respectfully request the Examiner to withdraw the rejection of claim 11 under 35 U.S.C. § 102(b) as being anticipated by the Nexus Specification.

Claims 12-25 depend, directly or indirectly, on claim 11 and thus are patentable for at least the reasons given above with respect to claim 11.

Claim 26 is also patentable because for similar reasons as given above with respect to claim 11, the Nexus Specification does not teach:

"a plurality of functional circuit module means, each being clocked by a clock that represents a different time domain, such that the plurality of functional circuit modules operate independently of each other with respect to time and each of the plurality of functional circuit modules having timestamping circuit means, the timestamping circuit means providing a timestamping message that indicates a point in time when a predetermined event occurs in a corresponding time domain out of a plurality of time domains," as required by claim 26.

Claim 27 depends from claim 26 and thus is patentable for at least the reasons given above with respect to claim 27.

Finally, newly added claims 46-49 are also patentable for at least the same reasons as given above with respect to claim 11, since each of them includes the patentable subject matter discussed above with respect to claim 11. Accordingly, Applicants request allowance of pending claims 11-27 and 46-49 over the Nexus Specification. The Office Action contains numerous statements characterizing the claims, the Specification, and the prior art. Regardless of whether such statements are addressed by Applicants, Applicants refuse to subscribe to any of these statements, unless expressly indicated by Applicants. Should issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 996-6839.

If Applicants have overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.

Law Department

Customer Number: 23125

By: /Ranjeev Singh/

SINGH, RANJEEV Attorney of Record Reg. No.: 47,093

Telephone: (512) 996-6839 Fax No.: (512) 996-6854